



# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for GSM and GSM EDGE base station applications with frequencies from 869 to 960 MHz. Suitable for TDMA, CDMA, and multicarrier amplifier applications.

### GSM Application

- Typical GSM Performance:  $V_{DD} = 26$  Volts,  $I_{DQ} = 600$  mA,  $P_{out} = 80$  Watts CW, Full Frequency Band (869-894 MHz or 921-960 MHz).  
 Power Gain — 18.5 dB  
 Drain Efficiency — 60%

### GSM EDGE Application

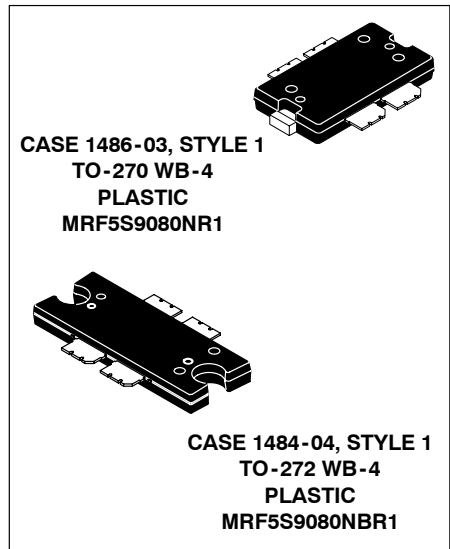
- Typical GSM EDGE Performance:  $V_{DD} = 26$  Volts,  $I_{DQ} = 550$  mA,  $P_{out} = 36$  Watts Avg., Full Frequency Band (869-894 MHz or 921-960 MHz).  
 Power Gain — 19 dB  
 Drain Efficiency — 42%  
 Spectral Regrowth @ 400 kHz Offset = -63 dBc  
 Spectral Regrowth @ 600 kHz Offset = -78 dBc  
 EVM — 2.5% rms
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 960 MHz, 80 Watts CW Output Power

### Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Qualified Up to a Maximum of 32  $V_{DD}$  Operation
- Integrated ESD Protection
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

**MRF5S9080NR1**  
**MRF5S9080NBR1**

**869-960 MHz, 80 W, 26 V**  
**GSM/GSM EDGE**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Storage Temperature Range	$T_{stg}$	- 65 to +150	°C
Operating Junction Temperature	$T_J$	200	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
Case Temperature 79°C, 80 W CW		0.50	
Case Temperature 80°C, 36 W CW		0.54	

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 26\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	500	nAdc

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 400\ \mu\text{Adc}$ )	$V_{GS(th)}$	2	2.8	3.5	Vdc
Gate Quiescent Voltage ( $V_{DS} = 26\text{ Vdc}$ , $I_D = 600\ \text{mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	3.5	3.9	4.5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 2\ \text{Adc}$ )	$V_{DS(on)}$	—	0.27	0.3	Vdc

**Dynamic Characteristics** (1)

Reverse Transfer Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{rss}$	—	1.8	—	pF
Output Capacitance ( $V_{DS} = 26\text{ Vdc} \pm 30\ \text{mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	600	—	pF

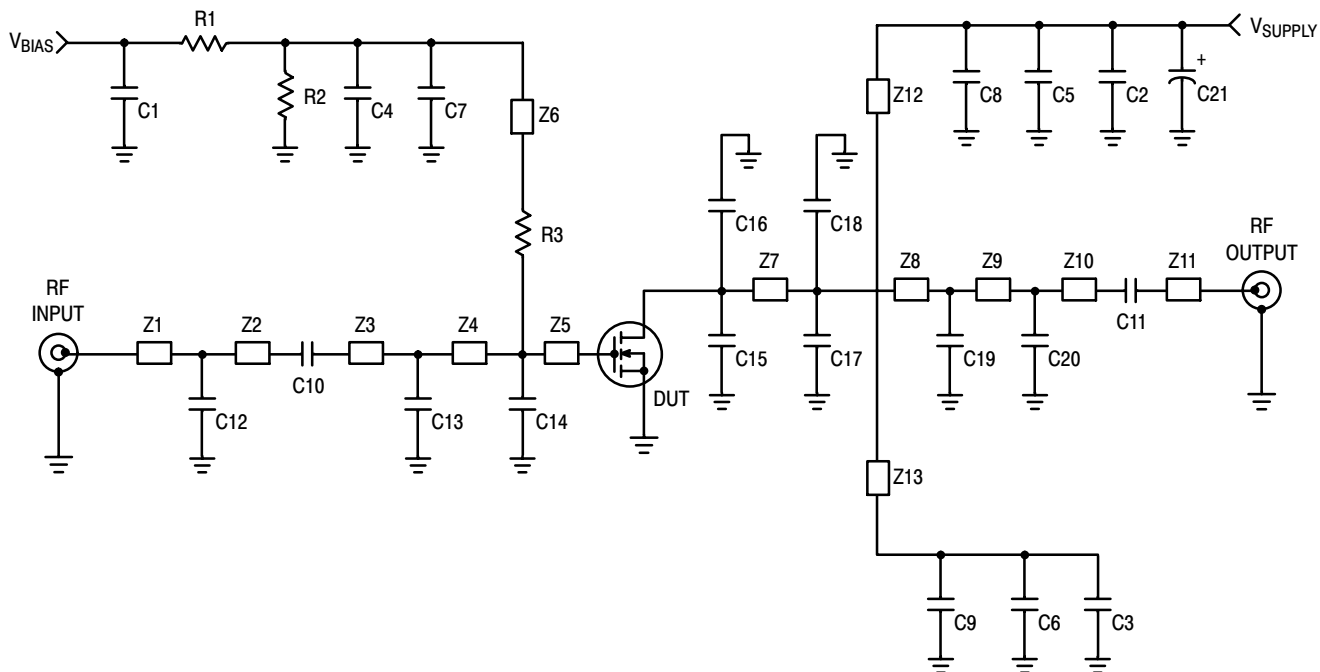
**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 26\text{ Vdc}$ ,  $I_{DQ} = 600\ \text{mA}$ ,  $P_{out} = 80\ \text{W CW}$ ,  $f = 960\ \text{MHz}$ 

Power Gain	$G_{ps}$	17	18.5	20	dB
Drain Efficiency	$\eta_D$	55	60	—	%
Input Return Loss	IRL	—	-15	-9	dB
$P_{out}$ @ 1 dB Compression Point	P1dB	80	90	—	W

**Typical GSM EDGE Performances** (In Freescale GSM EDGE Test Fixture, 50 ohm system)  $V_{DD} = 26\text{ Vdc}$ ,  $I_{DQ} = 550\ \text{mA}$ ,  $P_{out} = 36\ \text{W Avg.}$ , 869-894 MHz, 920-960 MHz GSM EDGE Modulation

Power Gain	$G_{ps}$	—	19	—	dB
Drain Efficiency	$\eta_D$	—	42	—	%
Error Vector Magnitude	EVM	—	2.5	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-63	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-77	—	dBc

1. Part is internally matched on input.



Z1 1.220" x 0.087" Microstrip  
 Z2 1.110" x 0.087" Microstrip  
 Z3 0.536" x 0.087" Microstrip  
 Z4 0.310" x 0.087" Microstrip  
 Z5 0.430" x 0.591" Microstrip  
 Z6 1.567" x 0.059" Microstrip  
 Z7 0.734" x 0.788" Microstrip

Z8 0.138" x 0.087" Microstrip  
 Z9 0.411" x 0.087" Microstrip  
 Z10 0.403" x 0.087" Microstrip  
 Z11 0.560" x 0.087" Microstrip  
 Z12, Z13 1.693" x 0.087" Microstrip  
 PCB Taconic TLX8-0300, 0.030",  $\epsilon_r = 2.55$

Figure 1. MRF5S9080NR1(NBR1) Test Circuit Schematic — 900 MHz

Table 6. MRF5S9080NR1(NBR1) Test Circuit Component Designations and Values — 900 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3	4.7 $\mu$ F Chip Capacitors (1812)	C4532X5R1H475MT	TDK
C4, C5, C6	10 nF 200B Chip Capacitors	200B103MW	ATC
C7, C8, C9	33 pF 600B Chip Capacitors	600B330JW	ATC
C10, C11	22 pF 600B Chip Capacitors	600B220FW	ATC
C12	1.8 pF 600B Chip Capacitor	600B1R8BW	ATC
C13	9.1 pF 600B Chip Capacitor	600B9R1BW	ATC
C14, C17, C18	8.2 pF 600B Chip Capacitors	600B8R2BW	ATC
C15, C16	10 pF 600B Chip Capacitors	600B100FW	ATC
C19	4.7 pF 600B Chip Capacitor	600B4R7BW	ATC
C20	3.6 pF 600B Chip Capacitor	600B3R6BW	ATC
C21	220 $\mu$ F, 63 V Electrolytic Capacitor, Axial	13668221	Philips
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors (1206)		
R3	10 $\Omega$ , 1/4 W Chip Resistor (1206)		

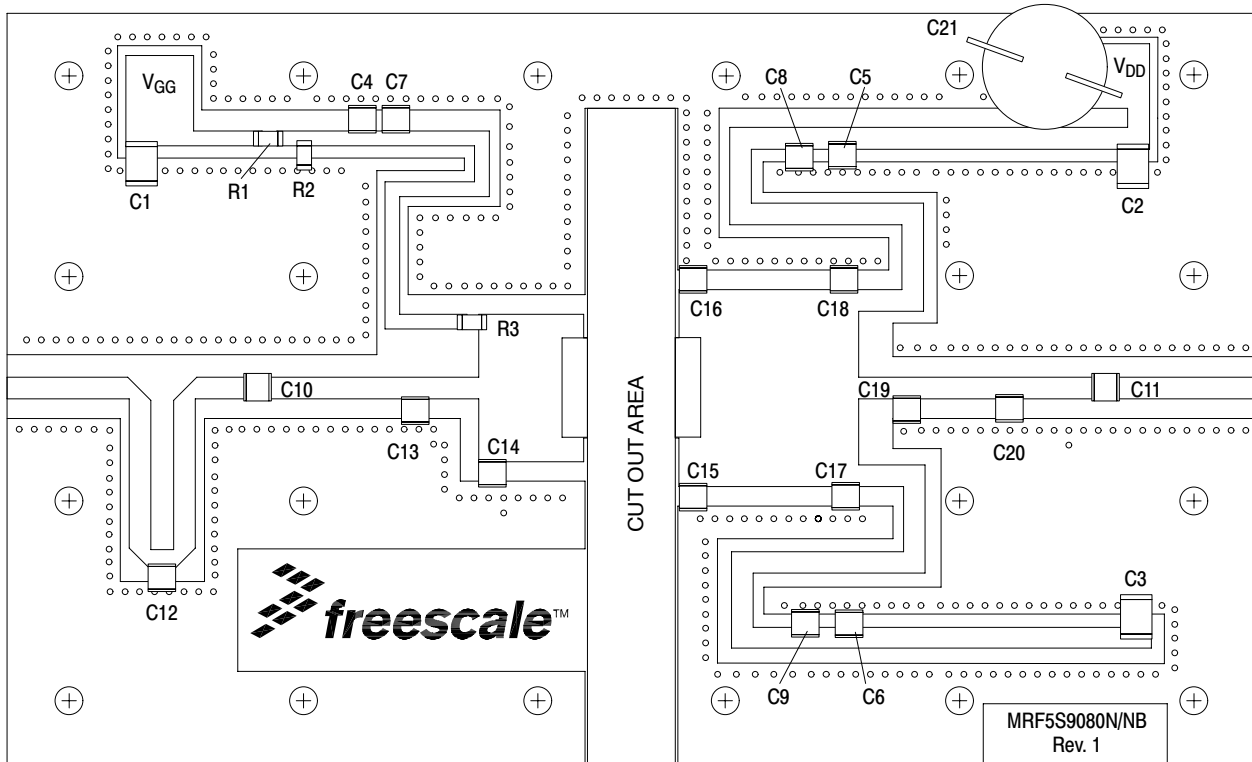


Figure 2. MRF5S9080NR1 (NBR1) Test Circuit Component Layout — 900 MHz

### TYPICAL CHARACTERISTICS - 900 MHz

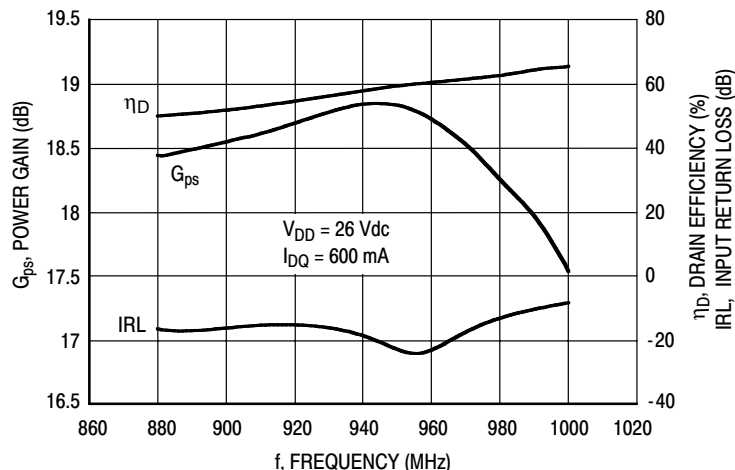


Figure 3. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @  $P_{out} = 80$  Watts CW

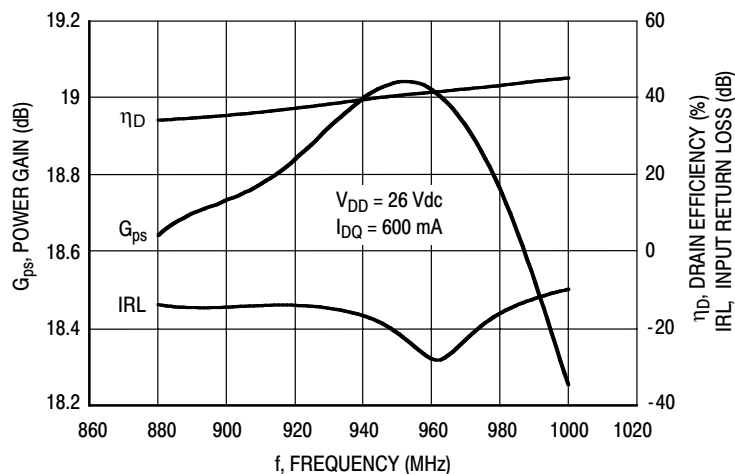


Figure 4. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @  $P_{out} = 36$  Watts CW

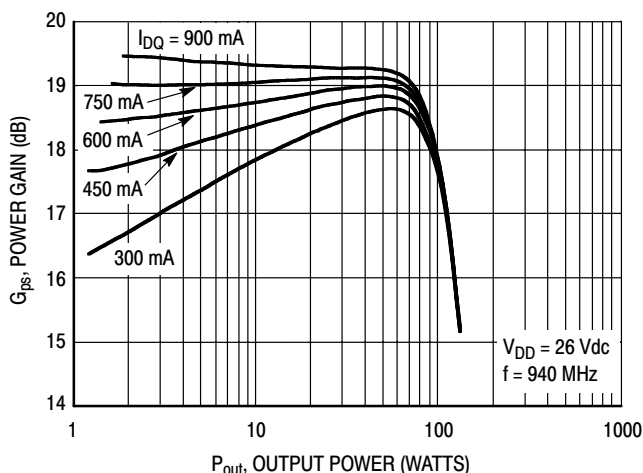


Figure 5. Power Gain versus Output Power

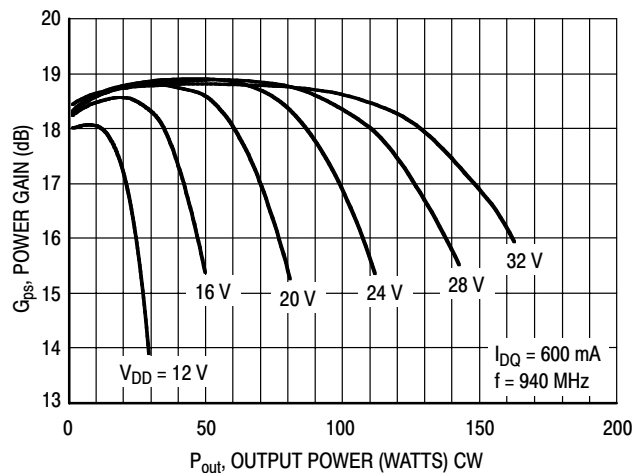
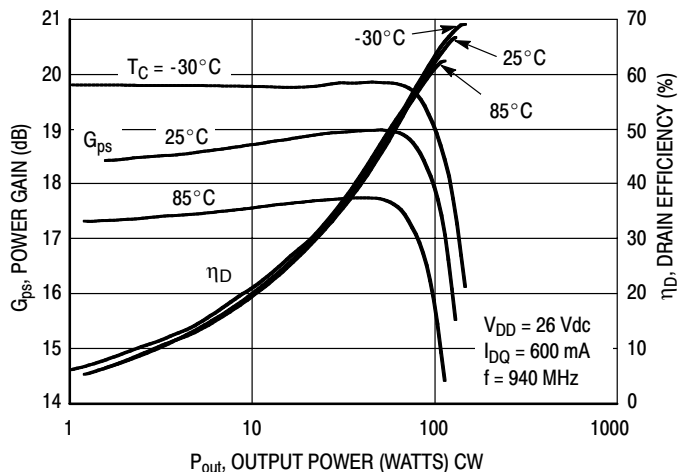
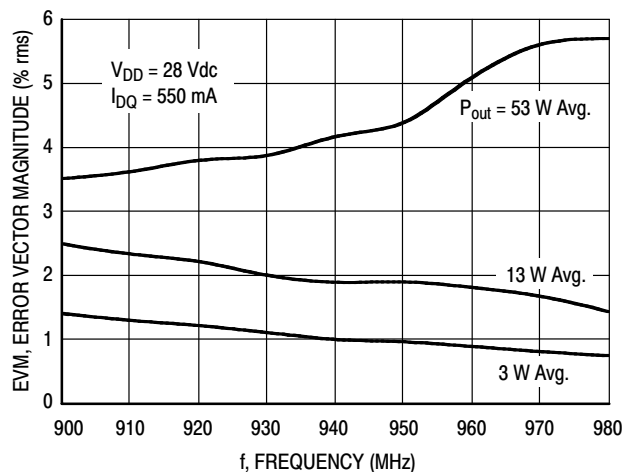


Figure 6. Power Gain versus Output Power

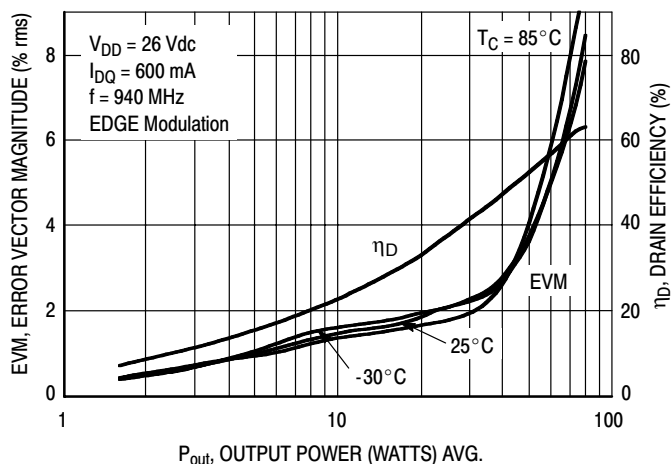
## TYPICAL CHARACTERISTICS - 900 MHz



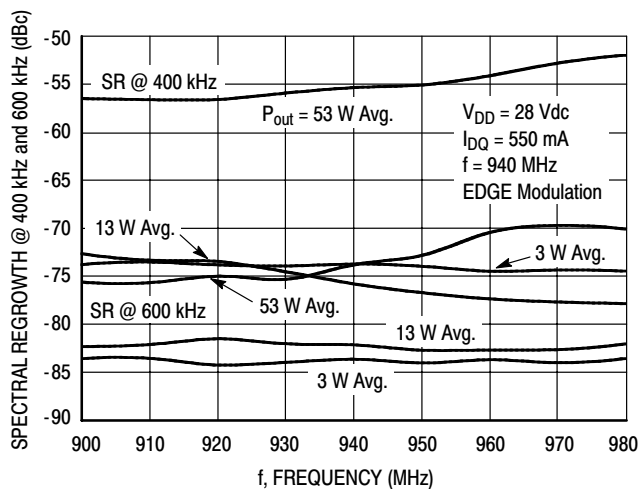
**Figure 7. Power Gain and Drain Efficiency versus CW Output Power**



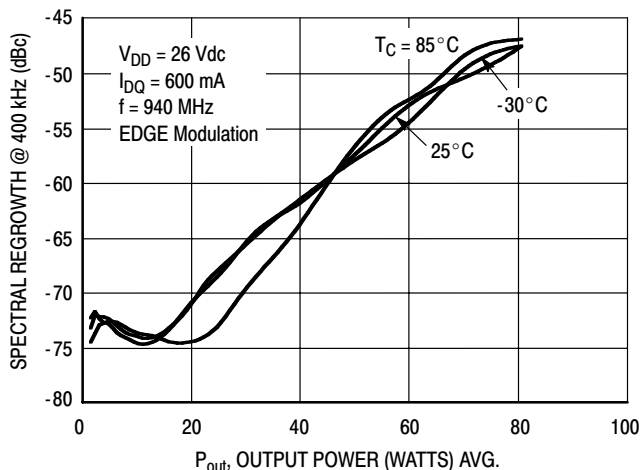
**Figure 8. EVM versus Frequency**



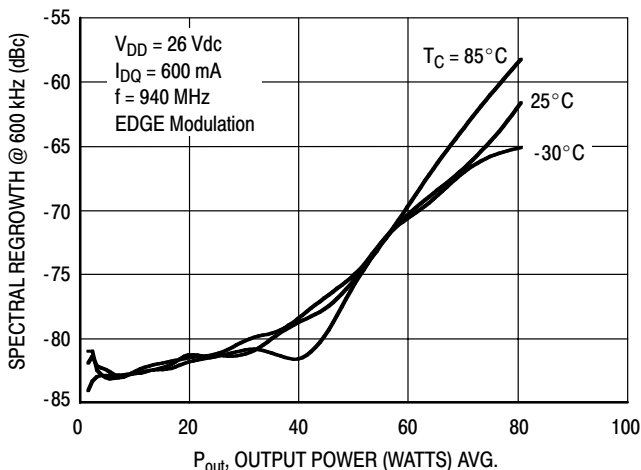
**Figure 9. EVM and Drain Efficiency versus Output Power**



**Figure 10. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency**

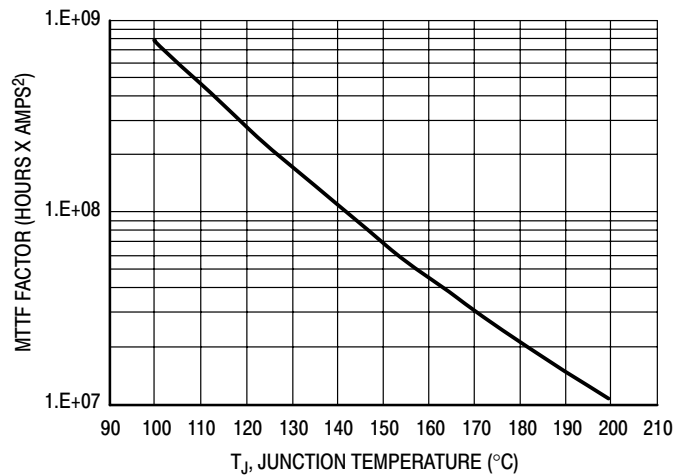


**Figure 11. Spectral Regrowth @ 400 kHz versus Output Power**



**Figure 12. Spectral Regrowth @ 600 kHz versus Output Power**

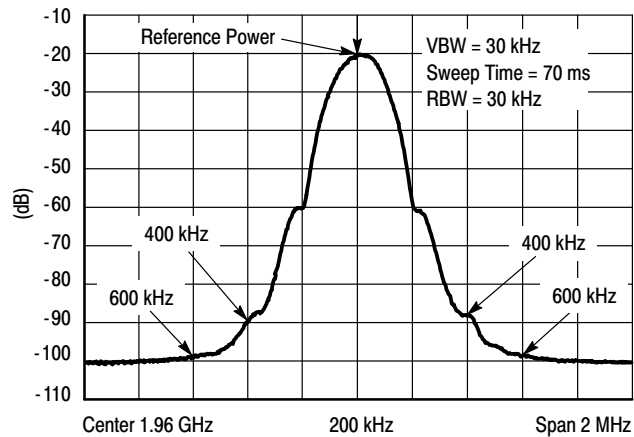
## TYPICAL CHARACTERISTICS



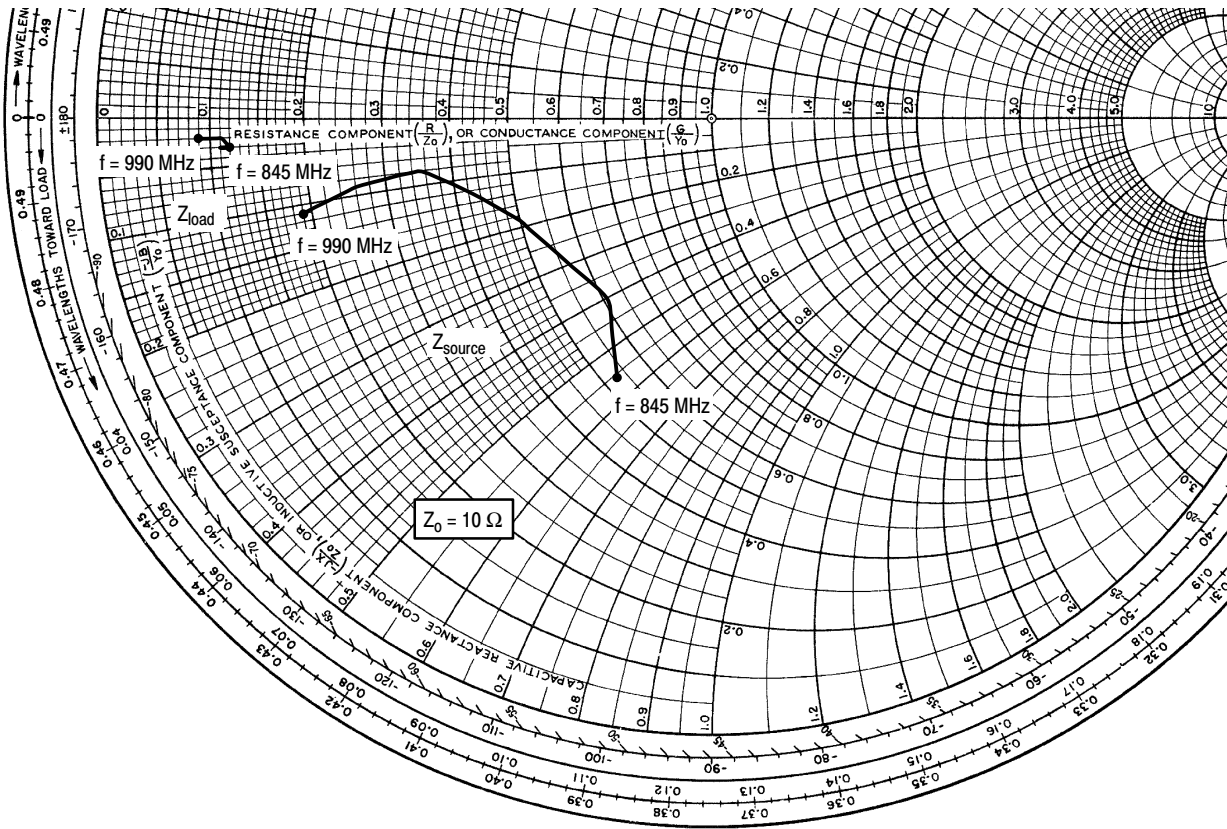
This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than  $\pm 10\%$  of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 13. MTTF Factor versus Junction Temperature**

## GSM TEST SIGNAL



**Figure 14. EDGE Spectrum**



$V_{DD} = 26 \text{ Vdc}$ ,  $I_{DQ} = 600 \text{ mA}$ ,  $P_{out} = 80 \text{ W CW}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
845	$5.31 - j5.59$	$1.18 - j0.34$
865	$6.07 - j4.16$	$1.09 - j0.29$
890	$5.05 - j1.99$	$1.22 - j0.29$
920	$3.47 - j0.81$	$1.10 - j0.21$
960	$2.64 - j0.88$	$1.05 - j0.15$
990	$1.89 - j1.14$	$0.91 - j0.18$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

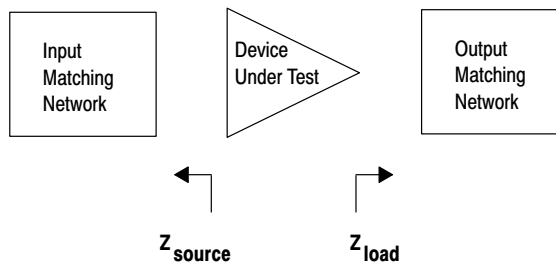
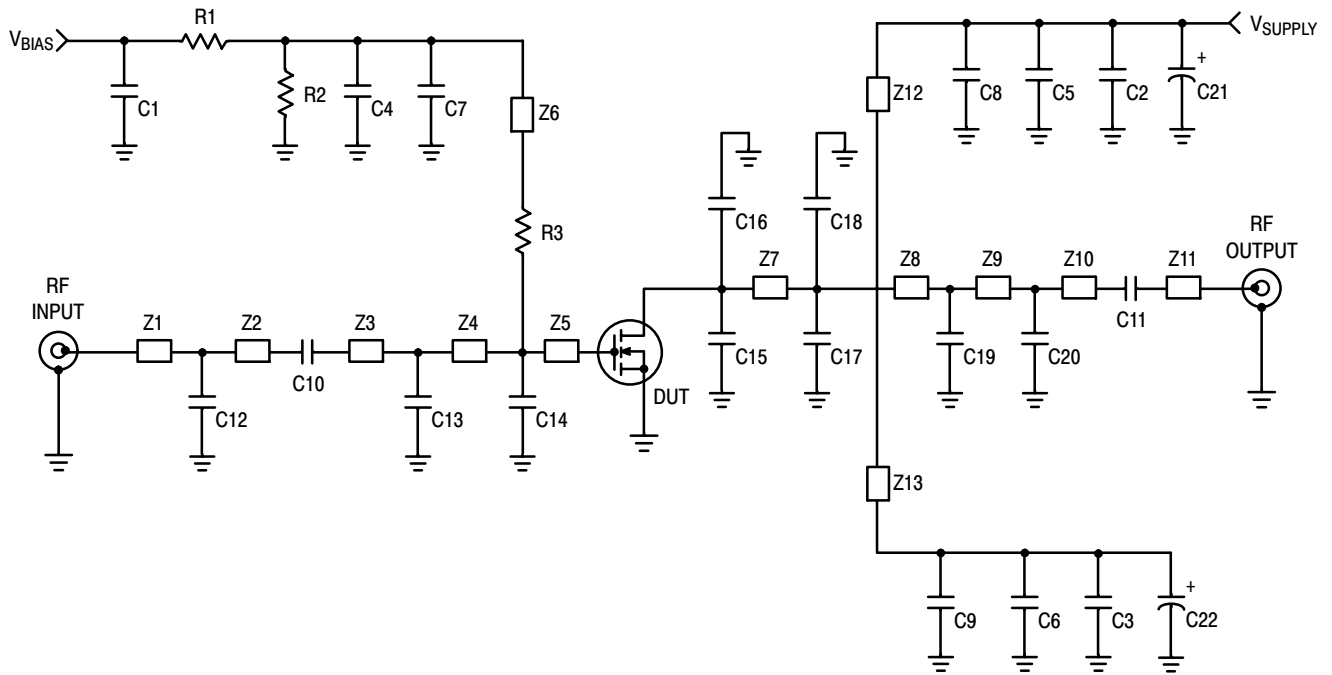


Figure 15. Series Equivalent Source and Load Impedance — 900 MHz





Z1	1.220" x 0.087" Microstrip	Z8	0.138" x 0.087" Microstrip
Z2	1.110" x 0.087" Microstrip	Z9	0.411" x 0.087" Microstrip
Z3	0.536" x 0.087" Microstrip	Z10	0.403" x 0.087" Microstrip
Z4	0.310" x 0.087" Microstrip	Z11	0.560" x 0.087" Microstrip
Z5	0.430" x 0.591" Microstrip	Z12, Z13	1.693" x 0.087" Microstrip
Z6	1.567" x 0.059" Microstrip	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$
Z7	0.734" x 0.788" Microstrip		

Figure 16. MRF5S9080NR1(NBR1) Test Circuit Schematic — 800 MHz

Table 7. MRF5S9080NR1(NBR1) Test Circuit Component Designations and Values — 800 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3	4.7 $\mu$ F Chip Capacitors (1812)	C4532X5R1H475MT	TDK
C4, C5, C6	10 nF 200B Chip Capacitors	200B103MW	ATC
C7, C8, C9	33 pF 600B Chip Capacitors	600B330JW	ATC
C10, C11	22 pF 600B Chip Capacitors	600B220FW	ATC
C12	1.8 pF 600B Chip Capacitor	600B1R8BW	ATC
C13	9.1 pF 600B Chip Capacitor	600B9R1BW	ATC
C14, C17, C18	8.2 pF 600B Chip Capacitors	600B8R2BW	ATC
C15, C16	10 pF 600B Chip Capacitors	600B100FW	ATC
C19	4.7 pF 600B Chip Capacitor	600B4R7BW	ATC
C20	3.6 pF 600B Chip Capacitor	600B3R6BW	ATC
C21, C22	220 $\mu$ F, 50 V Electrolytic Capacitors, Radial	678D227M050DM3D	Vishay
R1, R2	10 k $\Omega$ , 1/4 W Chip Resistors (1206)		
R3	10 $\Omega$ , 1/4 W Chip Resistor (1206)		

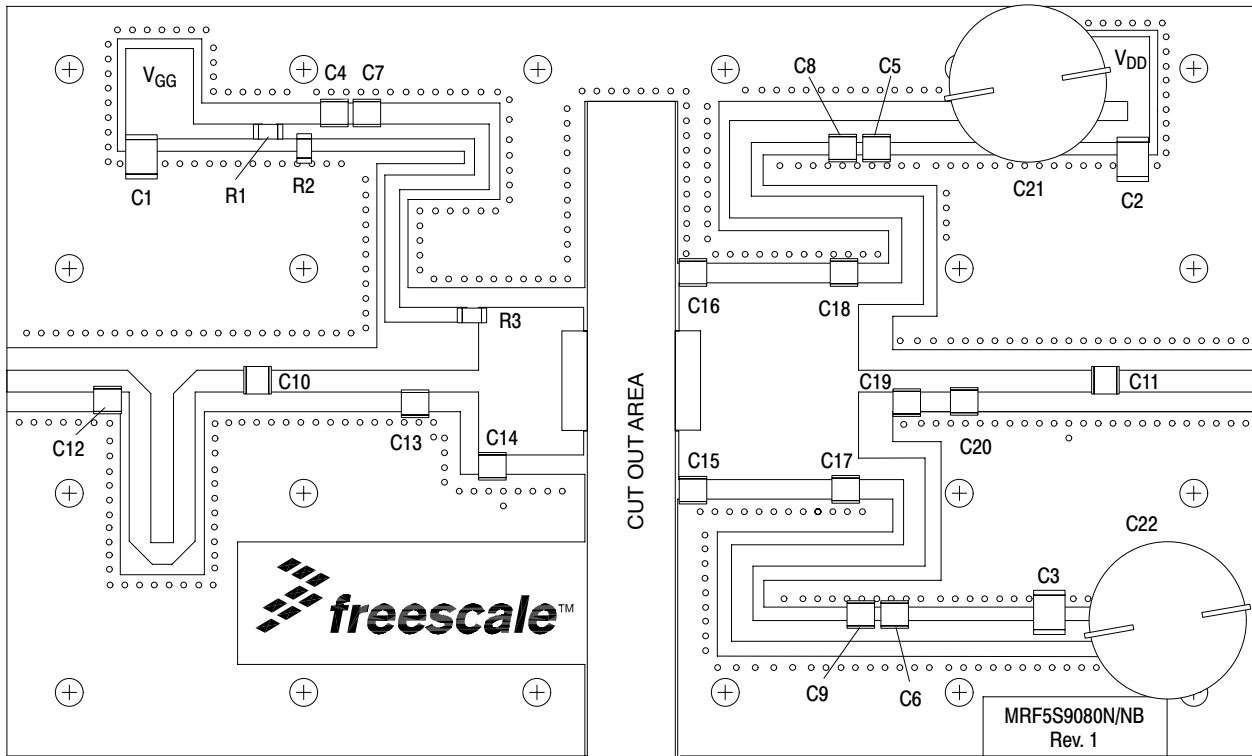


Figure 17. MRF5S9080NR1(NBR1) Test Circuit Component Layout — 800 MHz

### TYPICAL CHARACTERISTICS - 800 MHz

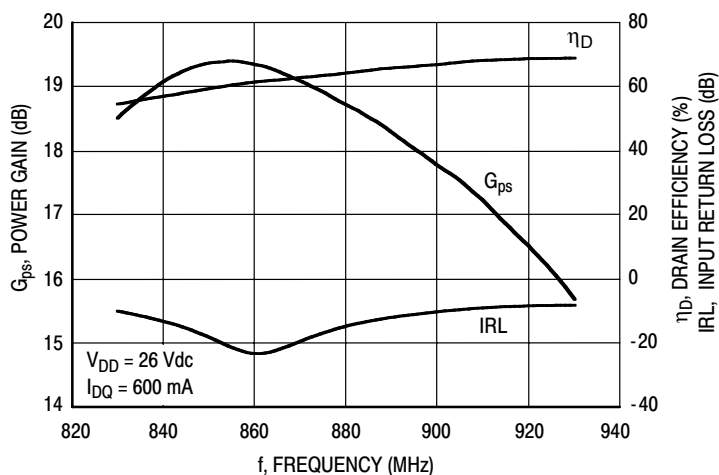


Figure 18. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @  $P_{out} = 80$  Watts

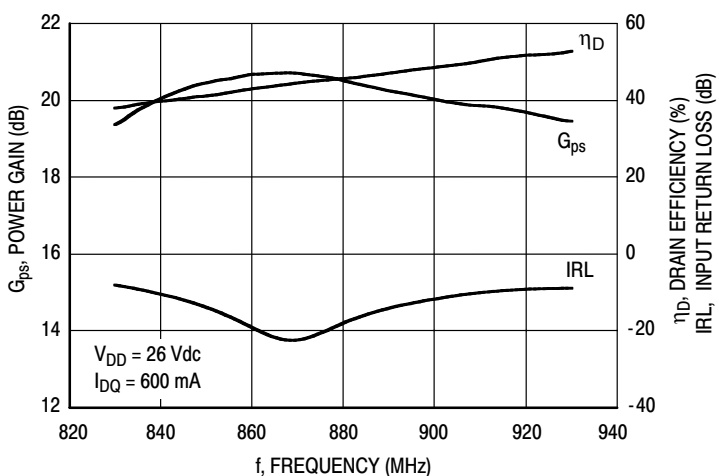


Figure 19. Power Gain, Input Return Loss and Drain Efficiency versus Frequency @  $P_{out} = 36$  Watts

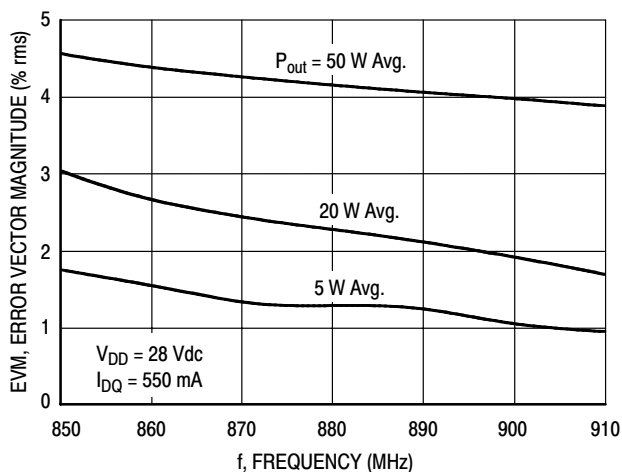


Figure 20. EVM versus Frequency

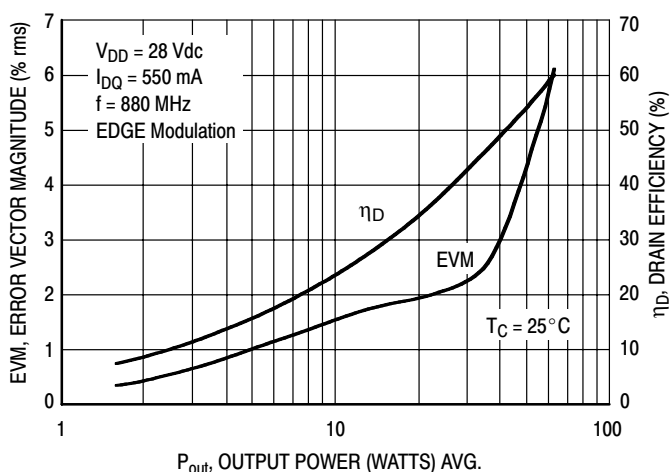
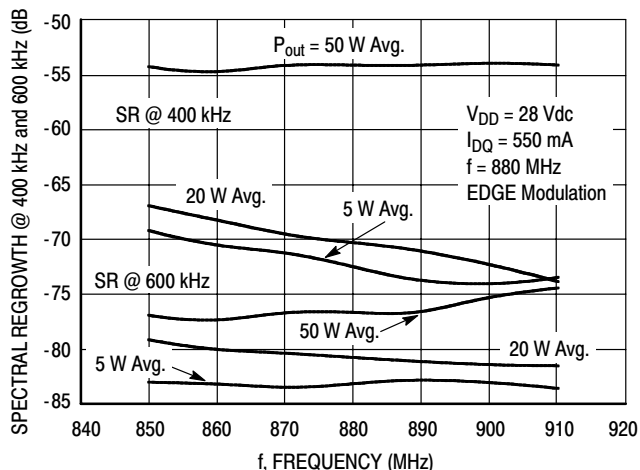
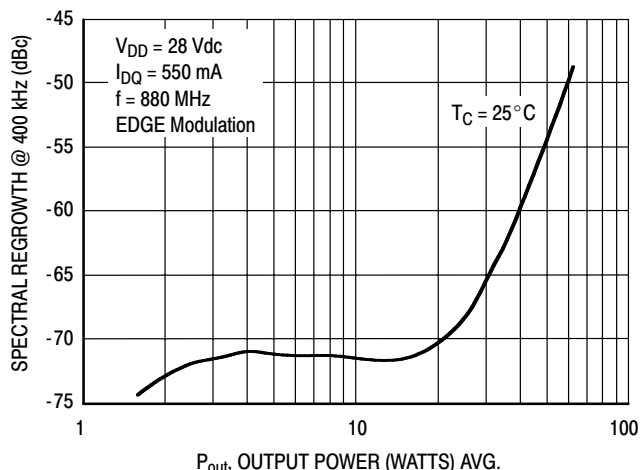


Figure 21. EVM and Drain Efficiency versus Output Power

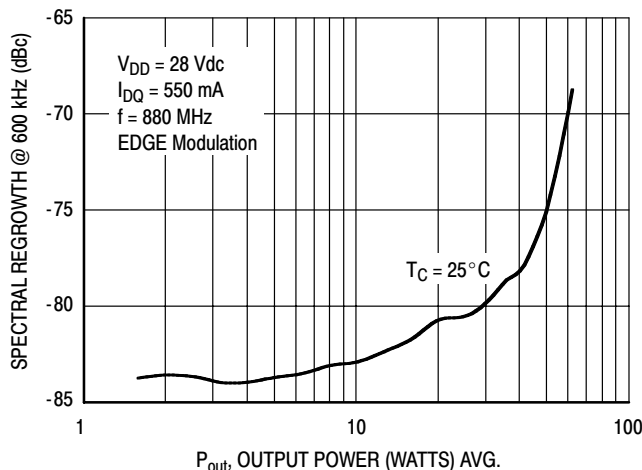
### TYPICAL CHARACTERISTICS - 800 MHz



**Figure 22. Spectral Regrowth at 400 kHz and 600 kHz versus Frequency**



**Figure 23. Spectral Regrowth @ 400 kHz versus Output Power**



**Figure 24. Spectral Regrowth @ 600 kHz versus Output Power**



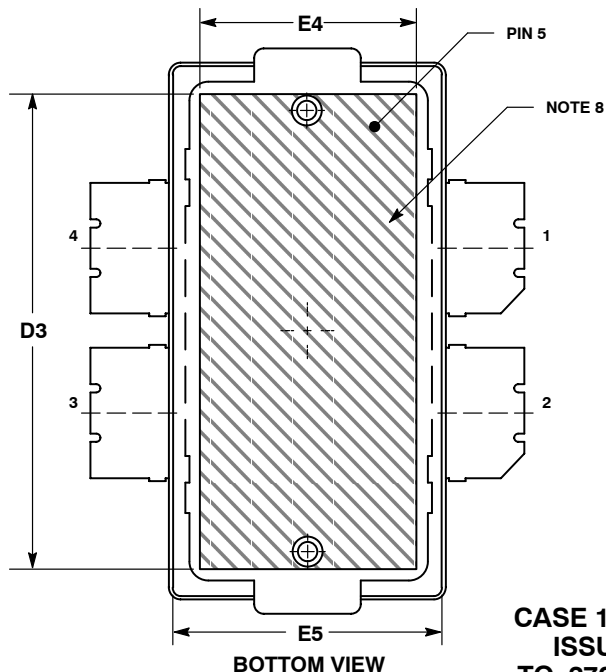
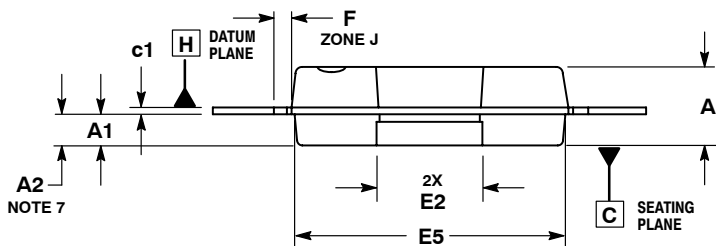
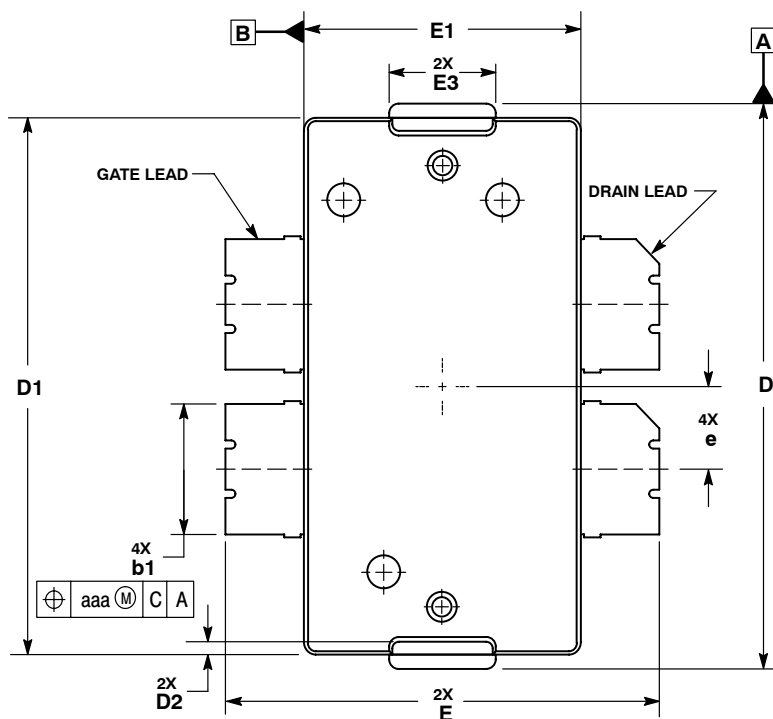
# NOTES

# NOTES



# NOTES

# PACKAGE DIMENSIONS



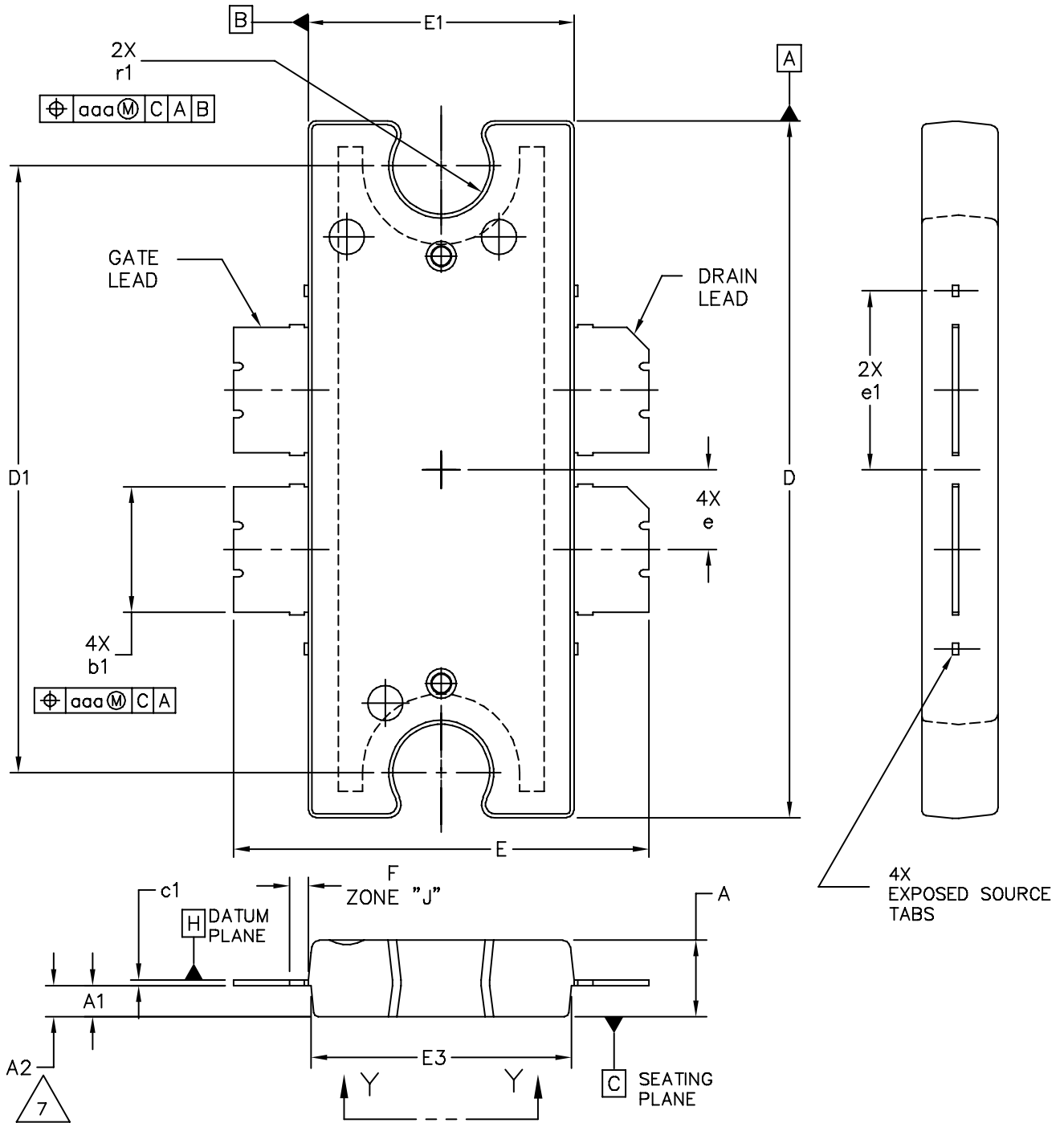
- NOTES:
1. CONTROLLING DIMENSION: INCH.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
  4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
  5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
  7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
  8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.712	.720	18.08	18.29
D1	.688	.692	17.48	17.58
D2	.011	.019	0.28	0.48
D3	.600	---	15.24	---
E	.551	.559	14	14.2
E1	.353	.357	8.97	9.07
E2	.132	.140	3.35	3.56
E3	.124	.132	3.15	3.35
E4	.270	---	6.86	---
E5	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
b1	.164	.170	4.17	4.32
c1	.007	.011	0.18	0.28
e	.106 BSC		2.69 BSC	
aaa	.004		0.10	

- STYLE 1:  
 PIN 1. DRAIN  
 2. DRAIN  
 3. GATE  
 4. GATE  
 5. SOURCE

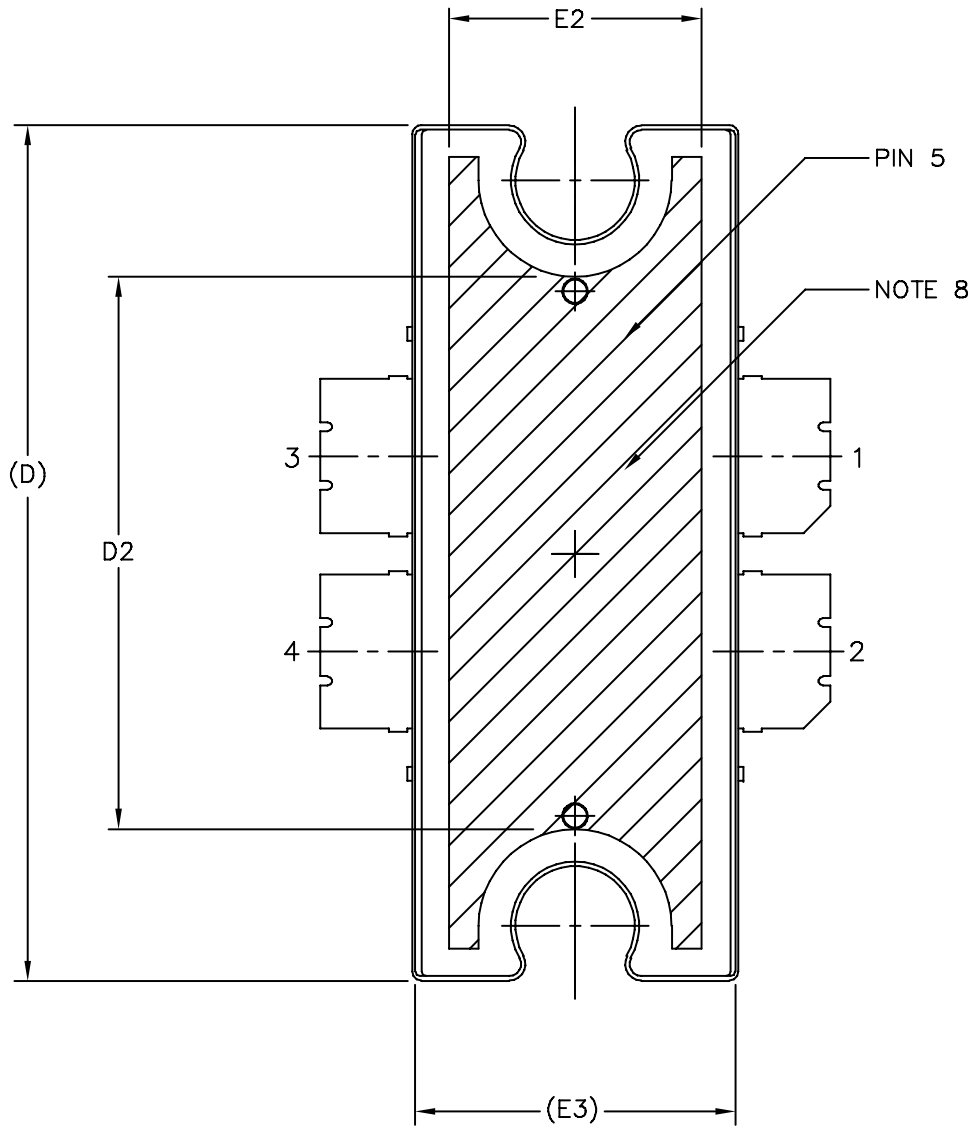
**CASE 1486-03  
 ISSUE C  
 TO-270 WB-4  
 PLASTIC  
 MRF5S9080NR1**





© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		<b>MECHANICAL OUTLINE</b>		PRINT VERSION NOT TO SCALE	
TITLE:  TO-272 4 LEAD, WIDE BODY			DOCUMENT NO: 98ASA10575D		REV: D
			CASE NUMBER: 1484-04		05 APR 2006
			STANDARD: NON-JEDEC		

MRF5S9080NR1 MRF5S9080NBR1



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: D	
	CASE NUMBER: 1484-04	05 APR 2006	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:

PIN 1 - DRAIN      PIN 2 - DRAIN  
 PIN 3 - GATE      PIN 4 - GATE  
 PIN 5 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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TITLE:  TO-272 4 LEAD WIDE BODY			DOCUMENT NO: 98ASA10575D		REV: D
			CASE NUMBER: 1484-04		05 APR 2006
			STANDARD: NON-JEDEC		

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